

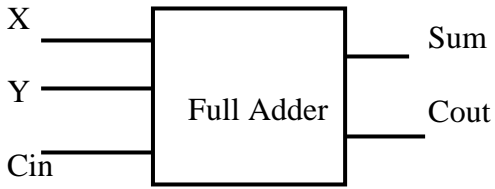
Read the instructions carefully before completing the exam. All answers must be shown on these pages - no attached pages will be graded. The Book referred to in this exam is the textbook for the class, Specifically Computer Organization and Design by Patterson and Hennessy. This exam is open book, open notes, and you may use a calculator. You may not use a computer, PDA, or a cell phone.

1. (15 points) Fill in the following table with hit or miss for the addresses in the order listed for the different types of cache, each of which has 4 data words in the cache and a block size of one. LRU is used for replacement.

Address	Direct mapped cache	Fully Associative	2 way set associative
1023	miss	miss	miss
4	miss	miss	miss
8	miss	miss	miss
7	miss	miss	miss
1023	miss	HIT	HIT
7	miss	HIT	HIT
9	miss	miss	miss
10	miss	miss	miss
8	HIT	miss	HIT
12	miss	miss	miss
1024	miss	miss	miss
4	miss	miss	miss
20	miss	miss	miss
4	miss	HIT	HIT
19	miss	miss	miss
	5 points	5 points	5 points

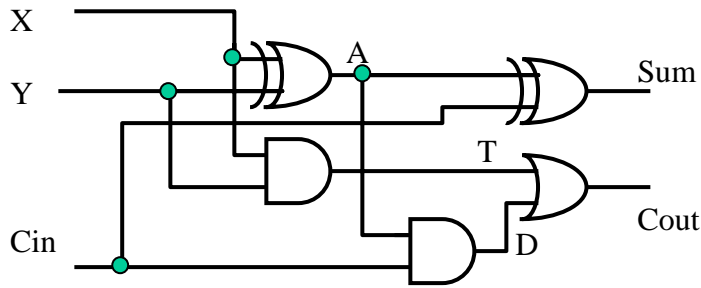
2. (4 Points) What is the Hit rate for the 2-way set associative cache? Note: the correct answer to this question (and the next two) is not based upon any incorrect entries in your table. Rather, the correct answer is based upon a completely correct Hit/Miss results table. Therefore, if you made mistakes in the Hit/Miss table you are not likely to get these three questions correct. $4/15 \approx 28\%$
3. (4 Points) What is the Hit rate for the direct mapped cache? $1/15 \approx 7\%$
4. (4 Points) What is the Hit rate for the fully associative cache? $3/15 \approx 20\%$

5. (13 Points) Complete the truth table for a Full Adder?



X	Y	Cin	Sum	Cout
0	0	0	<u>0</u>	<u>0</u>
0	0	1	<u>1</u>	<u>0</u>
0	1	0	<u>1</u>	<u>0</u>
0	1	1	<u>0</u>	<u>1</u>
1	0	0	<u>1</u>	<u>0</u>
1	0	1	<u>0</u>	<u>1</u>
1	1	0	<u>0</u>	<u>1</u>
1	1	1	<u>1</u>	<u>1</u>
0	0	z	<u>X</u>	<u>0</u>
0	1	z	<u>X</u>	<u>X</u>
1	0	z	<u>X</u>	<u>X</u>
1	1	z	<u>X</u>	<u>1</u>
z	z	z	<u>X</u>	<u>X</u>

6. (15 points) Complete the fault dictionary for the following circuit



Put a checkmark (✓) in the column for the vector(s) that detect the fault.

Q7	Q8		Vector = (XYCin)			
		Stuck-At Faults	000	010	100	111
•	•	X-S@0			✓	✓
•		X-S@1	✓	✓		
•	•	Y-S@0		✓		✓
•		Y-S@1	✓		✓	
•	•	Cin-S@0				✓
•		Cin-S@1	✓	✓	✓	
•		A-S@0		✓	✓	
•	•	A-S@1	✓			✓
•	•	T-S@0				✓
•	•	T-S@1	✓	✓	✓	
		D-S@0				
•	•	D-S@1	✓	✓	✓	
•	•	Sum-S@0		✓	✓	✓
•		Sum-S@1	✓			
•	•	Cout-S@0				✓
•	•	Cout-S@1	✓	✓	✓	

(Scoring = minus 1 point for each incorrect check or blank down to 0. Max score with all answers correct is 15; minimum score is 0 with 15 or more answers incorrect.)

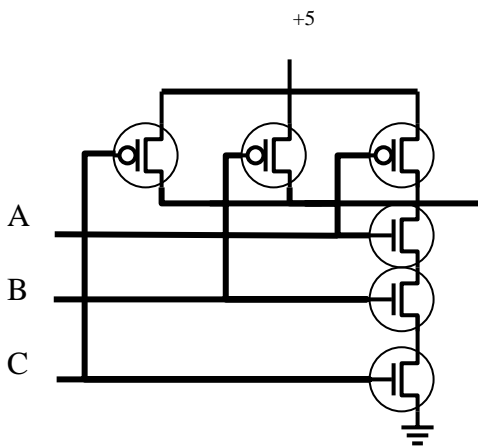
7. (5 points) What is the % fault coverage for the vector set of {(000), (010), (111)} applied to the above circuit?

15/16 ≈ 94% see Q7 in table

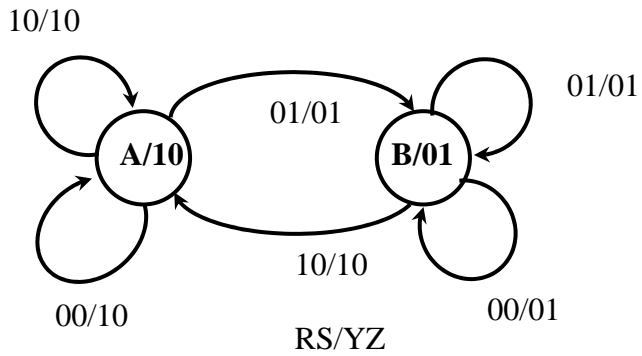
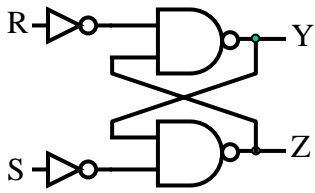
8. (5 points) What is the % fault coverage for the vector set of {(00z), (01z), (111)} applied to the above circuit?

10/16 ≈ 63% see Q8 in table

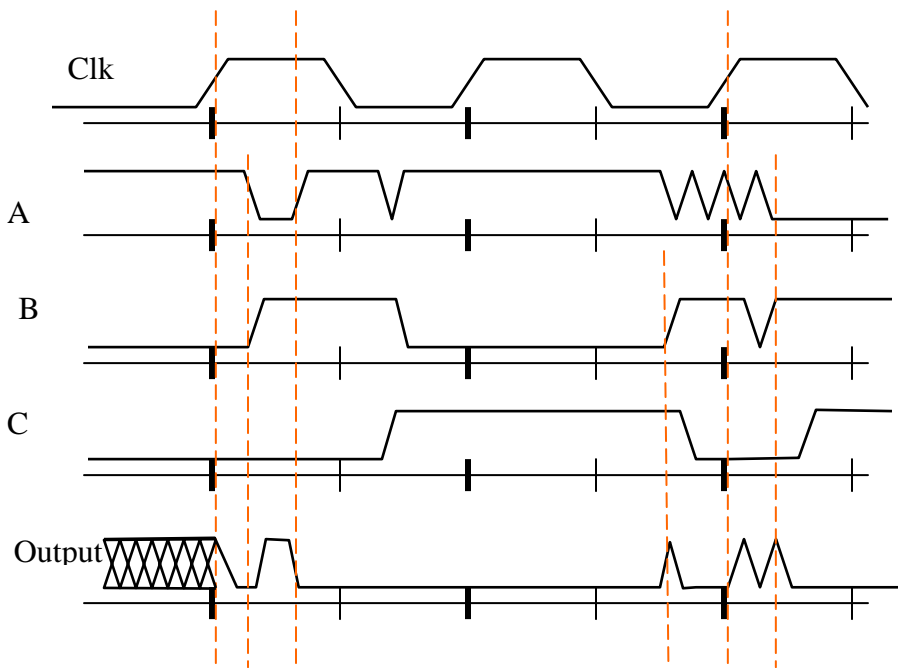
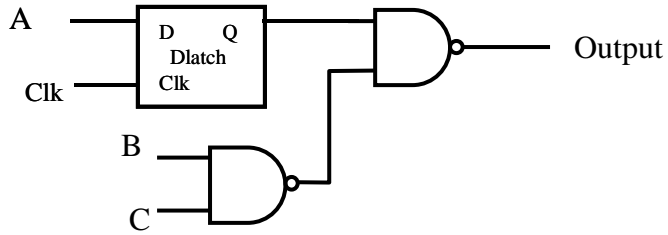
9. (5 points) Draw the transistor level circuit diagram for a 3-input NAND gate:



10. (5 points) Draw the state diagram for the following circuit:



11. (5 Points) Complete the timing diagram for the flowing circuit:



12. (5 points) Consider a direct mapped cache, in a system with a 32 bit address, a 32 bit data word, and 32,768 one word cache blocks. How many bits in the tag field?

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13. (5 points) Consider a direct mapped cache, in a system with a 32 bit address, a 32 bit data word, and 32,768 one word cache blocks. How many bits in the Main Memory?

$2^{37} = 137,438,953,472$

14. (5 points) Consider a direct mapped cache, in a system with a 32 bit address, a 32 bit data word, and 32,768 one word cache blocks. How many bits in the cache?

$50 * 32,768 = 1,638,400$

15. (5 points) Consider a 2-way set associative cache, in a system with a 32 bit address, a 32 bit data word, and 32,768 one word cache blocks, and the only overhead is the valid bit. How many bits in the cache?

1,671,168