

Read the instructions carefully before completing the exam. All answers must be shown on these pages - no attached pages will be graded. The Book referred to in this exam is the textbook for the class, specifically Computer Organization and Design by Patterson and Hennessy. This exam is open book, open notes, and you may use a calculator. You may not use a computer, PDA, or a cell phone.

1. (12 points) Fill in the following table about State Diagrams.

Number of Inputs	Number of State bits	Number of Outputs	Maximum number of States	Maximum number of total possible edges in the state diagram.
1	1	1	2	4
n_i	n_s	n_o	2^{n_s}	$2^{(n_s+n_i)}$
64	32	32	2^{32}	2^{96}
2	2	4	4	16
1	4	5	16	32
1	3	6	8	16

2. (15 points) Fill in the following table with hit or miss for the addresses in the order listed for the different types of cache, each of which has 16 data words in the cache and a block size of one. LRU is used for replacement.

Address	Direct mapped cache	Fully Associative	2 way set associative
1	miss	miss	miss
4	miss	miss	miss
8	miss	miss	miss
5	miss	miss	miss
20	miss	miss	miss
17	miss	miss	miss
9	miss	miss	miss
10	miss	miss	miss
11	miss	miss	miss
12	miss	miss	miss
27	miss	miss	miss
4	miss	Hit	miss
20	miss	Hit	miss
4	miss	His	Hit
19	miss	miss	miss
	5 points	5 points	5 points

3. (4 Points) What is the Hit rate for the 2-way set associative cache? Note: the correct answer to this question (and the next two) is not based upon any incorrect entries in your table. Rather, the correct answer is based upon a completely correct Hit/Miss results table. Therefore, if you made mistakes in the Hit/Miss table you are not likely to get these three questions correct.

$$1/15 = 6.7\%$$

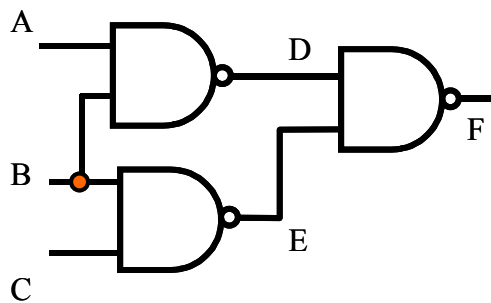
4. (4 Points) What is the Hit rate for the direct mapped cache?

$$0/15 = 0.0\%$$

5. (4 Points) What is the Miss rate for the fully associative cache?

$$12/15 = 80\%$$

6. (12 points) Complete the fault dictionary for the following circuit



Put a checkmark (✓) in the column for the vector(s) that detect the fault.

Stuck-At Faults	Vector = (ABC)							
	000	001	010	011	100	101	110	111
A-S@0							✓	
A-S@1			✓					
B-S@0				✓			✓	✓
B-S@1		✓			✓	✓		
C-S@0				✓				
C-S@1			✓					
D-S@0	✓	✓	✓		✓	✓		
D-S@1							✓	
E-S@0	✓	✓	✓		✓	✓		
E-S@1				✓				
F-S@0				✓			✓	✓
F-S@1	✓	✓	✓		✓	✓		

(Scoring = minus 1 point for each incorrect check or blank down to 0. Max score with all answers correct is 12; minimum score is 0 with 12 or more answers incorrect.)

7. (5 points) What is the % fault coverage for the vector set of {(000), (010), (111)} applied to the above circuit?

$$\underline{7/12 = 58\%}$$

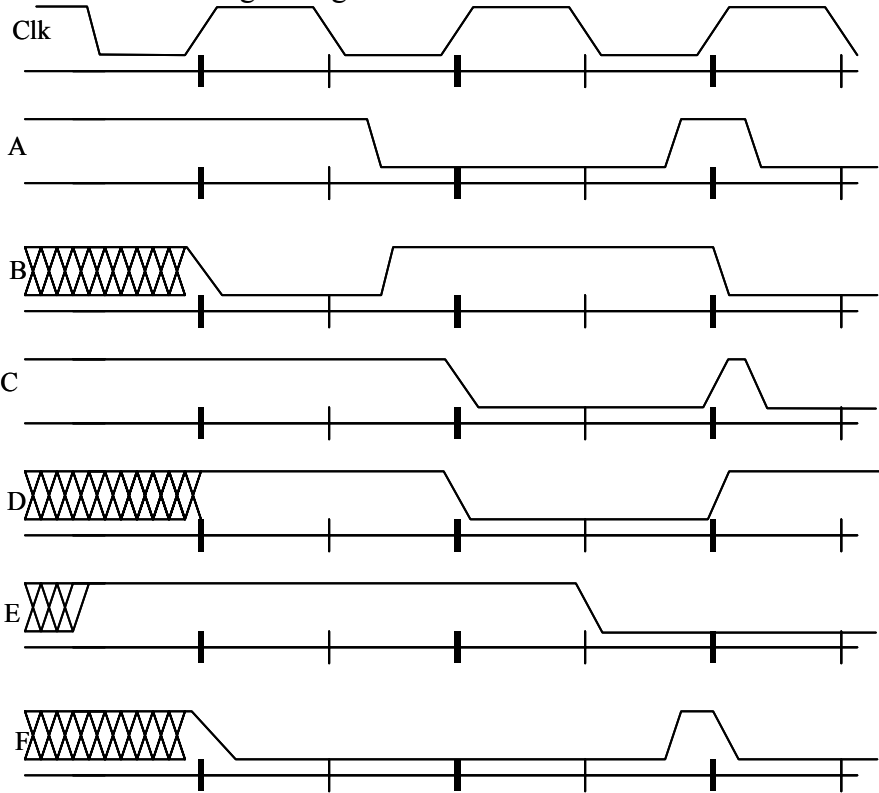
8. (5 points) What is a test vector set to get 100% fault coverage with 6 or fewer vectors?

{(010), (011), (110), and [(001) or (100) or (101)]}

The following multiple choice questions will be scored as 3 points (a plus 3) for each question that is correctly answered, -1 (a negative one) for an incorrect answer, and 0 for unanswered questions.

9. What does the PC stand for in the PC register?
- A) Politically Correct
 - B) Personal Computer
 - C) Program Code
 - D) Program Counter**
 - E) Progress Count
 - F) None of these choices.
10. Verilog gave the following error message:
- ```
Error! syntax error
"testbench.v", 1: /<- [Verilog]
```
- What caused this problem:
- A) The file testbench.v is missing
  - B) The fifth line of the file had a mistake
  - C) The file is missing a semicolon
  - D) A comment line is missing a /**
  - E) There is nothing wrong; this is a warning to be ignored.

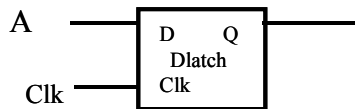
Consider the following timing waveforms:



11. This question refers to the timing diagram waveforms. For a two input NAND gate with waveform B as one input and waveform A as the other input, which waveform most closely represents the output?

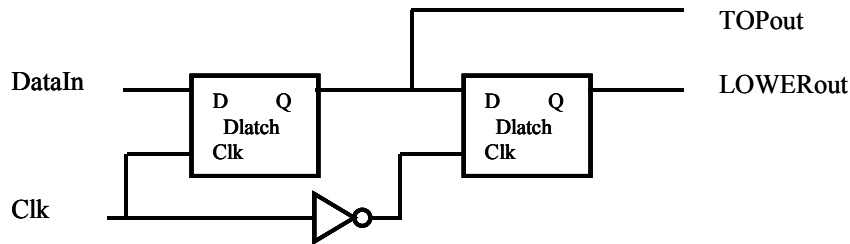
- A) None of the waveforms match the output.**
- B) Waveform B.
- C) Waveform C.
- D) Waveform D.
- E) Waveform E.
- F) Waveform F.

12. This question also refers to the timing diagram waveforms. For the following circuit (a positive level-sensitive D-latch), which waveform most closely represents the output?

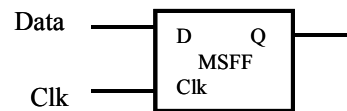


- A) None of the waveforms match the output.
- B) Waveform B.
- C) Waveform C.**
- D) Waveform D.
- E) Waveform E.
- F) Waveform F.

13. This question also refers to the timing diagram waveforms. For the following circuit (Two positive level sensitive D-latches) with waveform A as the DataIn and waveform B as the Clk (clock input), which waveforms most closely represent the two outputs?



- A) None of the waveforms match the outputs.  
 B) Waveform B matches TOPout and waveform C matches LOWERout.  
**C) Waveform C matches TOPout and waveform E matches LOWERout.**  
 D) Waveform F matches both outputs.  
 E) Waveform C matches TOPout and waveform D matches LOWERout.  
 F) Waveform F matches TOPout and waveform C matches LOWERout.
14. This question also refers to the timing diagram waveforms. For the following circuit (a positive-going edge-triggered Master-Slave Flip-Flop), with the Data input driven by waveform A and the Clk input driven by the waveform Clk, which waveform most closely represents the output?



- A) None of the waveforms match the output.  
 B) Waveform B.  
 C) Waveform C.  
**D) Waveform D.**  
 E) Waveform E.  
 F) Waveform F.
15. This question also refers to the timing diagram waveforms. For a two input AND gate with waveform B as one input and waveform A as the other input, which waveform most closely represents the output?
- A) None of the waveforms match the output.  
 B) Waveform B.  
 C) Waveform C.  
 D) Waveform D.  
 E) Waveform E.  
**F) Waveform F.**

Consider the following machine code instructions, where the format is:

| Opcode | Destination Register address | Operand A source register address | Operand B source register address | Immediate Value |
|--------|------------------------------|-----------------------------------|-----------------------------------|-----------------|
| 8 bits | 3 bits                       | 3 bits                            | 3 bits                            | 15 bits         |

The Instruction Register is 32 bits, the Program Counter is 32 bits, and register 0 is a constant 0.

| Instruction                                                   | Opcode |
|---------------------------------------------------------------|--------|
| Add A plus B                                                  | \$01   |
| A AND B                                                       | \$02   |
| A OR B                                                        | \$03   |
| NOT B                                                         | \$04   |
| NOP                                                           | \$AA   |
| A XOR B                                                       | \$F1   |
| A AND Immediate Value                                         | \$F2   |
| Jump to Immediate Value                                       | \$F3   |
| Logical Shift Left of A by Immediate Constant number of bits. | \$F4   |
| Stop or Halt                                                  | \$F5   |

The Following instructions are executed:

| Memory Address | Contents   |
|----------------|------------|
| \$0000000f     | \$043C0000 |
| \$00000010     | \$F4E68010 |
| \$00000011     | \$F267001B |
| \$00000012     | \$F14F8000 |
| \$00000013     | \$F3BD8024 |
| \$00000014     | \$AA000024 |
| \$00000015     | \$F1650018 |
| \$00000016     | \$F3BD826A |
| \$00000017     | \$AA00026A |
| \$00000018     |            |
| \$00000019     |            |
| \$0000001A     |            |
| \$0000001B     |            |
| \$0000001C     |            |
| \$0000001D     |            |
| \$0000001E     |            |
| \$0000001F     |            |
| \$00000020     |            |
| \$00000021     |            |
| \$00000022     |            |
| \$00000023     | \$F300000F |
| \$00000024     | \$AA00001F |
| \$00000025     | \$AA317F00 |
| \$00000026     | \$F5FF8000 |
| \$00000027     | \$AA000000 |
| \$00000028     |            |

16. At the beginning of the program execution, which registers have a value of \$00000000?

- A) **Register 0**
- B) Register 1
- C) Register 2
- D) Register 3
- E) Register 4
- F) Register 5
- G) Register 6
- H) Register 7
- I) All of the registers
- J) None of the registers

17. At the beginning of the program execution, which registers have a value of \$FFFFFFFF?

- A) Register 0
- B) Register 1
- C) Register 2
- D) Register 3
- E) Register 4
- F) Register 5
- G) Register 6
- H) Register 7
- I) All of the registers
- J) **None of the registers**

18. At the end of the program execution, which registers have a value of \$FFFFFFFF?

- A) Register 0
- B) **Register 1**
- C) Register 2
- D) Register 3
- E) Register 4
- F) Register 5
- G) Register 6
- H) Register 7
- I) All of the registers
- J) None of the registers

19. At the end of the program execution, which registers have a value of \$00000000?

- A) **Register 0**
- B) Register 1
- C) Register 2
- D) Register 3
- E) Register 4
- F) Register 5
- G) Register 6
- H) Register 7
- I) All of the registers
- J) None of the registers

20. At the end of the program execution, what is the value in the PC Register?

- A) \$00000000
- B) \$FFFFFFFF
- C) \$00000028
- D) \$00000027**
- E) \$00000026
- F) \$FFFF0027
- G) \$0000FFFF
- H) \$F5FF9000
- I) All of these values :-)
- J) None of these values.

21. At the end of the program execution, what is the value in the Register 2?

- A) \$00000000
- B) \$FFFFFFFF
- C) \$00000028
- D) \$00000027
- E) \$00000026
- F) \$FFFF0027
- G) \$0000FFFF
- H) \$F5FF9000
- I) All of these values ☺
- J) None of these values.**