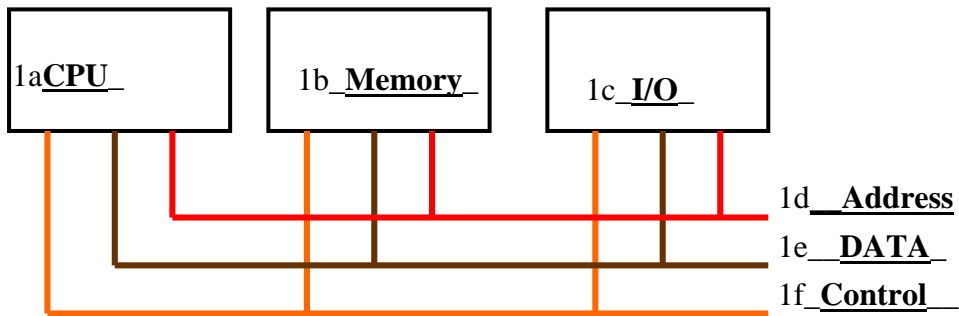


Read the instructions carefully before completing the exam. All answers must be shown on these pages - no attached pages will be graded. The Book referred to in this exam is the textbook for the class, Specifically Computer Organization and Design by Patterson and Hennessy. This exam is open book, open notes, and you may use a calculator. You may not use a computer, PDA, or a cell phone.



1. (6 points) Label the diagram of the three major components of any digital computer system and the three busses connecting them



2. (12 points) Fill in the following table about State Diagrams.

Number of Inputs	Number of State bits	Number of Outputs	Maximum number of States	Maximum number of edges out of each state
1	1	6	<u>2</u>	<u>2</u>
1	2	5	<u>4</u>	<u>2</u>
2	2	3	<u>4</u>	<u>4</u>
3	2	4	<u>4</u>	<u>8</u>
2	3	2	<u>8</u>	<u>4</u>
3	3	1	<u>8</u>	<u>8</u>

Consider a computer with a PC of 16 bits, an Ireg of 16 bits, and 32 general-purpose registers of 16 bits each.

3. (2 points) The data bus has 16 bits.
4. (2 points) The address bus has 16 bits.
- ⊗ 5. (2 points) The control bus has variable or unknown bits.

The following multiple choice questions will be scored as 3 points (a plus 3) for each question that is correctly answered, -1 (a negative one) for an incorrect answer, and 0 for unanswered questions.

6. For a completely specified state diagram, how many edges exit each state for a circuit with 2 inputs?
A) 1
B) 2
C) 3
D) 4
E) Cannot be determined from the information given.
F) None of the above.
7. Consider the following Verilog Code
module KK(MM, NN, OO, PP);
 input MM, NN;
 output OO, PP;
 xor(OO, MM, NN);
 and(PP, MM, NN);
endmodule

What type of HDL is this?

- A) This is structural HDL
- B) This is behavioral HDL**
- C) This is a test bench
- D) This is not HDL at all, but it is Pseudo-code
- E) All of the above
- F) None of the above

8. Consider the following Verilog Code

```

module KK(MM, NN, OO, PP);
  input MM, NN;
  output OO, PP;
  jxor inst1(.OO(OO), .MM(MM),.NN(NN));
  jand inst2(.PP(PP),.MM( MM),.NN( NN));
endmodule

```

What type of HDL is this?

- A) **This is structural HDL**
- B) This is behavioral HDL
- C) This is a test bench
- D) This is not HDL at all, but it is Pseudo-code
- E) All of the above
- F) None of the above

⊗

9. Verilog gave the following error message:

```

Error! syntax error
"testbench.v", 1: /<-      [Verilog]

```

What caused this problem:

- A) The file testbench.v is missing
- B) The fifth line of the file had a mistake
- C) The file is missing a semicolon
- D) **A comment line is missing a /**
- E) There is nothing wrong, this is a warning to be ignored.

10. Consider the following Verilog Code

```

module cell(Alice, Bob, Eve, Wally);
  input ports are Alice and Bob and are one bit each;
  Output ports are Eve and Wally and are one bit each;
  Set Eve to the parity of Alice and Bob;
  set Wally to the true when both Alice and Bob are true;
endmodule

```

What type of HDL is this?

- A) This is structural HDL
- B) This is behavioral HDL
- C) This is a test bench
- D) **This is not HDL at all, but it is Pseudo-code**
- E) All of the above
- F) None of the above

11. The instruction fetch step uses which bus (or buses)?
- A) Data Bus
 - B) Address Bus
 - C) Control Bus
 - D) All three**
 - E) A and B only
 - F) None of the buses
12. The general-purpose register file connects to which bus (or buses)?
- A) Data Bus
 - B) Address Bus
 - C) Control Bus
 - D) All three
 - E) A and C only**
 - F) A and B only
 - G) None of the buses
13. The PC register drives which bus (or buses)?
- A) Data Bus
 - B) Address Bus**
 - C) Control Bus
 - D) All three
 - E) A and C only
 - F) A and B only
 - G) None of the buses
14. How many States can be represented by 4 memory bits?
- A) 5
 - B) 16
 - C) 35
 - D) 28
 - E) 32
 - F) All four of A, B, D, and E
 - G) Both A and B**
 - H) None of these
15. How many bytes can be addressed by 16 address bits for a memory that has 16 bit words?
- A) 1024
 - B) 17179869184
 - C) 1048576
 - D) 131072**
 - E) 65536
 - F) None of the above

The following True/False questions are worth 2 points each. Circle T for True or F for False for your answer.

16. F The CPU Block presented in the lectures contains the output component mentioned in the Book.
17. T The instruction step of getting the operands requires that the General Purpose Register address be decoded.
18. T The instruction step of saving the results requires that the General Purpose Register address be decoded.
19. T During the instruction fetch step, the value for the address bus comes from the Program Counter.
20. F During the instruction fetch step, the value for the address bus comes from the Address Register.
- ☠
21. F During the instruction fetch step, the address for the Data Bus comes from the Ireg.
- 😊😊
22. T or F During the get operands step, the address for the address bus comes from the Address Register.
23. F During the get operands step, the address for the address bus comes from the control unit.
24. F During the save results step, the address bus always goes to be used by the memory block.
25. T The first time an address is output from the CPU it is always a positive integer.
26. F The second time an address is output from the CPU it is sometimes a negative integer.
- ☹
27. F For a 16 bit address field in an instruction and a 32 bit address bus, one half of the address space can be directly addressed.
- 😊😊
28. T A byte is eight bits.
- 😊😊
29. F A nibble is five bits.



30. F The same bit pattern could be used as a binary number, a register, an ASCII code, and a machine code instruction.



31. T The CPU Block presented in the lectures contains the Control component mentioned in the Book.

32. F The CPU Block presented in the lectures contains the input component mentioned in the Book.

33. T The Instruction Fetch (IF) step of an instruction puts the value contained in the Program Control Register (PC Reg) onto the address bus.

34. T Instruction decoding is sometimes (usually) part of the Instruction Fetch (IF) step of an instruction.

35. F The execute/alu step of getting the operands requires that the General Purpose Register address be decoded.

36. F In a Load/Store architecture, the operands for addition are loaded directly from main memory.

37. F In a Load/Store architecture, the results bus does not put values into a general-purpose register (GP Reg).

38. T The CPU Block presented in the lectures contains the data path component mentioned in the Book.

The following two questions are bonus questions. They will only add to your score up to a total test score of 100, so no overall test score over 100. Each question is worth 4 points.

39. How many bits in a MIPS instruction?

32

40. How many bits in the address field of a load word MIPS instruction?

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