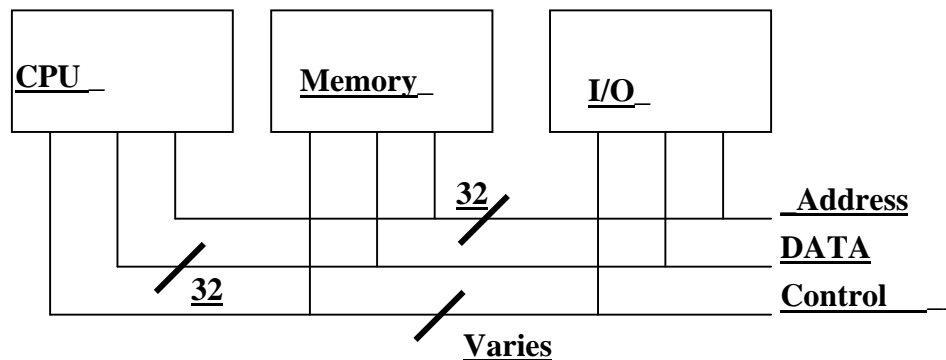


Read the instructions carefully before completing the exam. All answers must be shown on these pages - no attached pages will be graded. The Book referred to in this exam is the textbook for the class, Specifically Computer Organization and Design by Patterson and Hennessy. This exam is open book, open notes, and you may use a calculator.

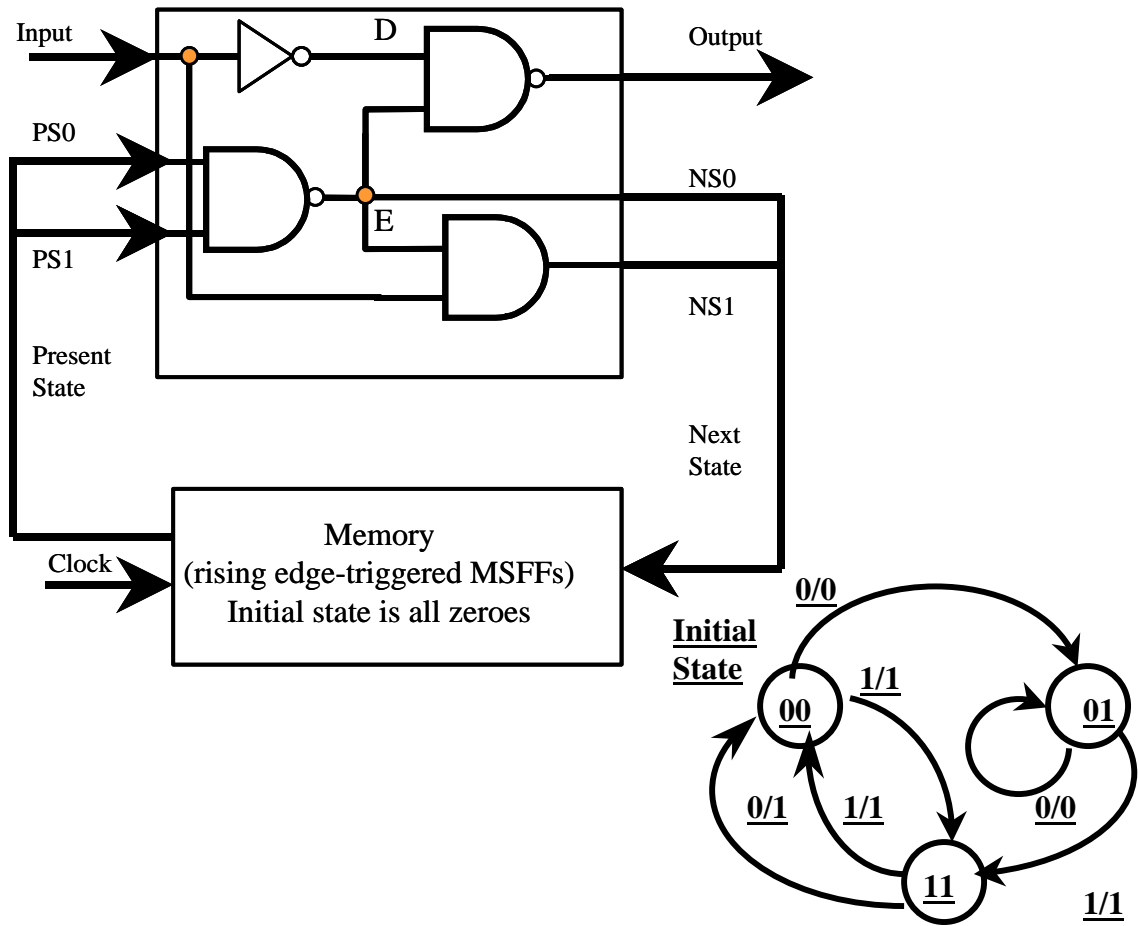
1. (6 points) Fill in the following table with Hex numbers for the appropriate representation (include leading zeroes).

Decimal Value	32 bit sign-magnitude	8 bit sign-magnitude	32 bit ones complement	8 bit ones complement	8 bit twos complement
38	<u>h00000026</u>	<u>h26</u>	<u>h00000026</u>	<u>h26</u>	<u>h26</u>
28	<u>h0000001C</u>	<u>h1C</u>	<u>h0000001C</u>	<u>h1C</u>	<u>h1C</u>
-10	<u>h8000000A</u>	<u>h8A</u>	<u>hFFFFFFF5</u>	<u>hF5</u>	<u>hF6</u>
16	<u>h00000010</u>	<u>h10</u>	<u>h00000010</u>	<u>h10</u>	<u>h10</u>
13	<u>h0000000D</u>	<u>h0D</u>	<u>h0000000D</u>	<u>h0D</u>	<u>h0D</u>
-3	<u>h80000003</u>	<u>h83</u>	<u>hFFFFFFFC</u>	<u>hFC</u>	<u>hFD</u>

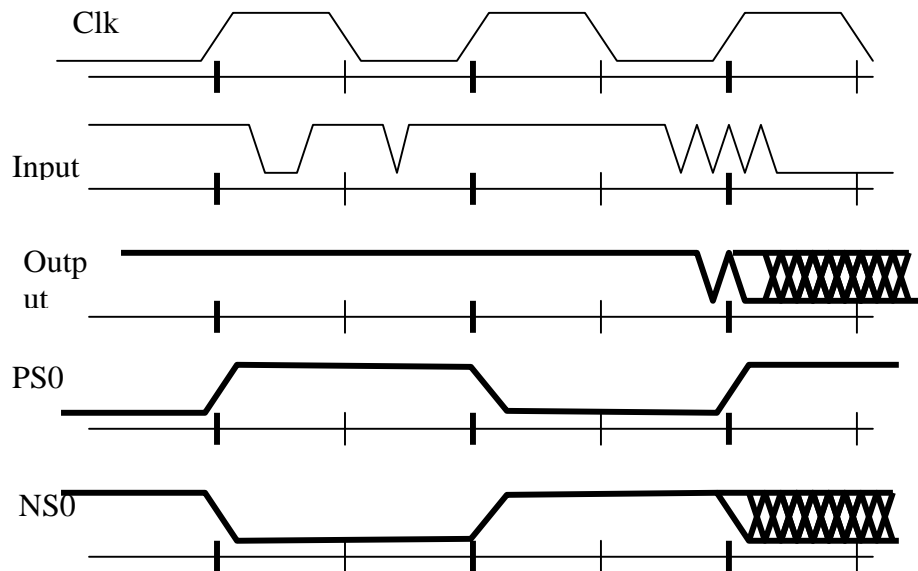
2. (6 points) For a 32 bit processor, with a 32 bit address, Draw the block diagram of a digital computer system showing the three blocks connected to three busses, with the busses labeled with a slash and the appropriate number of bits.



3. (20 Points) Draw a state diagram for the following circuit:

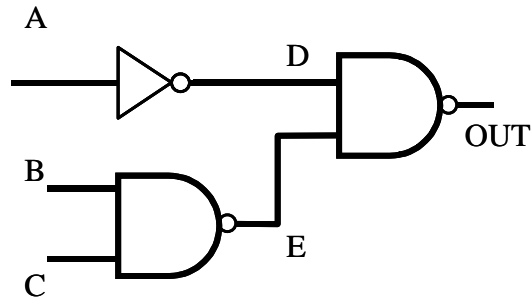


4. (20 points) Complete the following timing diagram for the sequential circuit in the previous question:



5. (2 points) How many Stuck at faults are possible in the following circuit:

12



6. (20 points) Complete the fault dictionary for the above circuit

Vector = (ABC)

	000	001	010	011	100	101	110	111
Asa0					✓	✓	✓	
Asa1	✓	✓	✓					
Bsa0				✓				
Bsa1		✓						
Csa0				✓				
Csa1			✓					
Dsa0	✓	✓	✓					
Dsa1					✓	✓	✓	
Esa0	✓	✓	✓					
Esa1				✓				
outSa0				✓	✓	✓	✓	✓
outSa1	✓	✓	✓					

7. (4 points) What is the % fault coverage for the vector set of {(000), (010), (111)} applied to the above circuit?

50%

8. (4 points) What is a test vector set to get 100% fault coverage with 5 or fewer vectors?

{(001),(010),(011),(100)}

Each of the following true/false questions is worth 2 points.

9. **T** During the instruction fetch step, the address for the cache comes from the Program Counter.
10. **F** During the instruction fetch step, the address for the cache comes from the Address Register.
11. **F** During the instruction fetch step, the address for the cache comes from the tags.
12. **T** During the get operands step, the address for the cache comes from the Address Register.
13. **F** During the get operands step, the address for the cache comes from the tags.
14. **F** During the save results step, the address for the cache comes from the index.
15. **T** The first time an address is accessed it is always a cache miss.
16. **F** The second time an address is accessed it is always a cache hit.
17. **F** For a 1024 line direct mapped cache and a 32 bit address, the index is 22 bits.