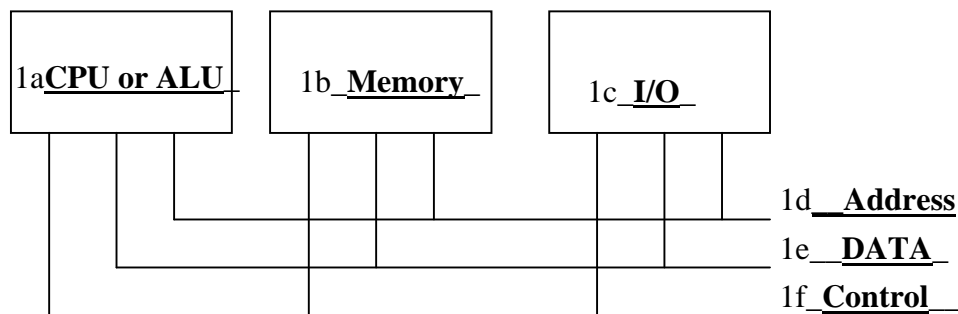
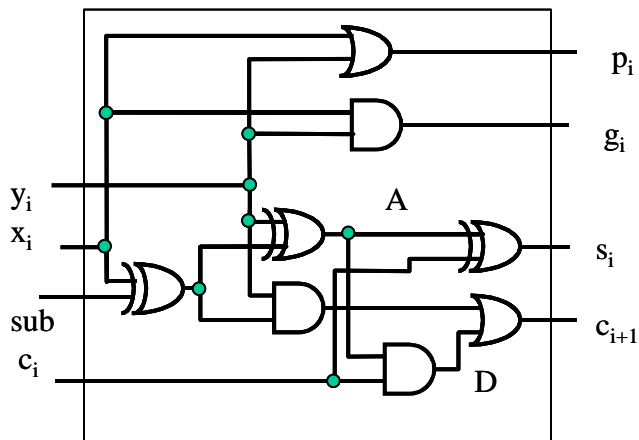


Read the instructions carefully before completing the exam. All answers must be shown on these pages - no attached pages will be graded. The Book referred to in this exam is the textbook for the class, Specifically Computer Organization and Design by Patterson and Hennessy. This exam is open book, open notes, and you may use a calculator.

- (3 points) Label the diagram of the three major components of any digital computer system and the three busses connecting them



Consider the following single bit very simple ALU circuit.



- (2 points) For the specific ALU implementation described, how many gate delays are there from input  $x_i$  to output  $s_i$ ? 3
- (2 points) For the specific ALU implementation shown, how many gate delays are there from input  $y_i$  to output  $s_i$ ? 2

4. (3 points) For the specific ALU implementation shown, how many gate delays are there for the longest path? 4
5. (4 points) For the specific ALU implementation shown, and a two level LACG, how many gate delays are there for the path from x0 to Carry out? 3
6. (4 points) For the 4 bits in series of the specific ALU implementation shown, how many gate delays are there for the path from x0 to Carry out (that is c4)? 10

7. (15 points) Fill in the following table with Hex numbers for the appropriate representation.

Decimal Value	32 bit sign-magnitude	8 bit sign-magnitude	32 bit ones complement	8 bit ones complement	8 bit twos complement
127	<u>0000007F</u>	<u>7F</u>	<u>0000007F</u>	<u>7F</u>	<u>7F</u>
-126	<u>8000007E</u>	<u>FE</u>	<u>FFFFFF81</u>	<u>81</u>	<u>82</u>
15	<u>0000000F</u>	<u>0F</u>	<u>0000000F</u>	<u>0F</u>	<u>0F</u>
-15	<u>8000000F</u>	<u>8F</u>	<u>FFFFFFF0</u>	<u>F0</u>	<u>F1</u>
31	<u>0000001F</u>	<u>1F</u>	<u>0000001F</u>	<u>1F</u>	<u>1F</u>
-64	<u>80000040</u>	<u>C0</u>	<u>FFFFFFBF</u>	<u>BF</u>	<u>C0</u>

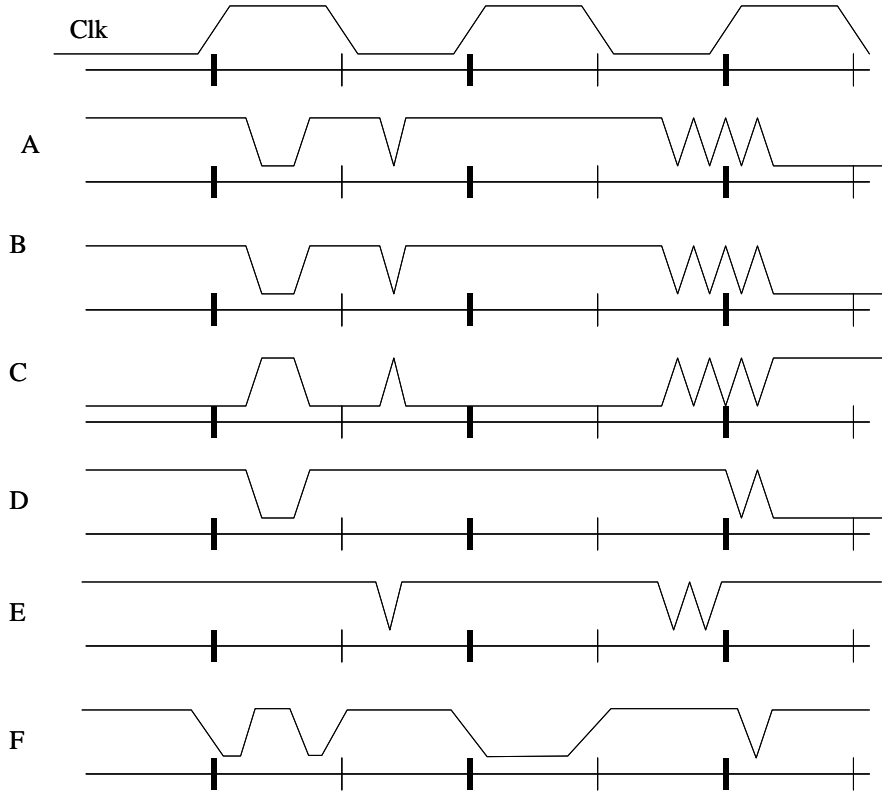
8. (9 points) Fill in the following table about State Diagrams.

Number of Inputs	Number of State bits	Number of Outputs	Maximum number of States	Maximum number of edges out of each state	Maximum number of total possible edges in the state diagram.
1	1	1	<u>2</u>	<u>2</u>	<u>4</u>
1	2	2	<u>4</u>	<u>2</u>	<u>8</u>
2	1	3	<u>2</u>	<u>4</u>	<u>8</u>
2	2	4	<u>4</u>	<u>4</u>	<u>16</u>
3	2	5	<u>4</u>	<u>8</u>	<u>32</u>
4	3	6	<u>8</u>	<u>16</u>	<u>128</u>

The following multiple choice questions will be scored as 3 points (a plus 3) for each question that is correctly answered, -1 (a negative one) for an incorrect answer, and 0 for unanswered questions.

9. For a completely specified state diagram, how many edges exit each state for a circuit with 2 inputs?
- A) 1
  - B) 2
  - C) 3
  - D) 4**
  - E) Cannot be determined from the information given.
  - F) None of the above.
10. How many States can be represented by 5 memory bits?
- A) 5
  - B) 16
  - C) 35
  - D) 28
  - E) 32
  - F) All four of A, B, D, and E**
  - G) None of these
11. For the given ALU circuit, What path has the longest delay (that is the highest gate delay count)?
- A) x to c**
  - B) x to s
  - C) y to c
  - D) y to s
  - E) c to c
  - F) c to s
  - G) None of the above.

Consider the following timing diagram waveforms.



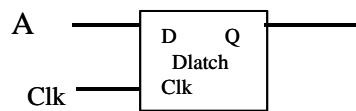
12. This question refers to the timing diagram waveforms. For a two input NAND gate with the waveform labeled Clk as one input and the waveform labeled A as the other input, which waveform most closely represents the output.

- A) None of the waveforms match the output.
- B) Waveform B.
- C) Waveform C.
- D) Waveform D.
- E) Waveform E.
- F) Waveform F.**

13. This question also refers to the timing diagram waveforms. For a two input OR gate with the waveform labeled Clk as one input and the waveform labeled A as the other input, which waveform most closely represents the output.

- A) None of the waveforms match the output.
- B) Waveform B.
- C) Waveform C.
- D) Waveform D.
- E) Waveform E.**
- F) Waveform F.

14. This question also refers to the timing diagram waveforms. For the following circuit (a positive level sensitive D-latch) which waveform most closely represents the output?



- A) None of the waveforms match the output.  
B) Waveform B.  
C) Waveform C.  
**D) Waveform D.**  
E) Waveform E.  
F) Waveform F.
15. How many bytes can be addressed by 32 address bits for a memory that has 32 bit words?  
A) 1024  
**B) 17179869184**  
C) 1073741824  
D) 2147483648  
E) 4294967296  
F) None of the above
16. How many words can be addressed by 32 address bits for a memory that has 32 bit words?  
A) 1024  
B) 256  
C) 1073741824  
D) 2147483648  
**E) 4294967296**  
F) None of the above
17. How many bits can be addressed by 32 address bits for a memory that has 32 bit words?  
A) 1024  
B) 256  
C) 1073741824  
D) 2147483648  
E) 4294967296  
**F) None of the above**

18. How many words can be addressed by 10 address bits for a memory that has 8 bit words?

- A) 1024**
- B) 2048
- C) 4096
- D) 8192
- E) 4294967296
- F) None of the above

19. How many bits can be addressed by 10 address bits for a memory that has 8 bit words?

- A) 1024
- B) 2048
- C) 4096
- D) 8192**
- E) 4294967296
- F) None of the above

20. How many bytes can be addressed by 10 address bits for a memory that has 8 bit words?

- A) 1024**
- B) 2048
- C) 4096
- D) 8192
- E) 4294967296
- F) None of the above

The following True/False questions are worth 2 points each. Circle T for True or F for False for your answer.

21. **T** A byte is eight bits.
22. **T** A nibble is four bits.
23. **T** The same bit pattern could be used as a binary number, an ASCII code, and a machine code instruction.
24. **T** The CPU Block presented in the lectures contains the Control component mentioned in the Book.
25. **F** The CPU Block presented in the lectures contains the input component mentioned in the Book.
26. **T** The Instruction Fetch (IF) step of an instruction puts the value contained in the Program Control Register (PC Reg) onto the address bus.
27. **T** Instruction decoding is sometimes (usually) part of the Instruction Fetch (IF) step of an instruction.
28. **T** The instruction step of getting the operands requires that the General Purpose Register address be decoder.
29. **F** In a Load/Store architecture, the operands for addition are loaded directly from main memory.
30. **F** In a Load/Store architecture, the results bus does not put values into a general purpose register (GP Reg).
31. **T** **F** The CPU Block presented in the lectures contains the data path component mentioned in the Book.